P2004,0327

Patent Claims

1. Process to generate a structured layer (10A) with the following process steps:

A) at least one layer (10) is arranged on a substrate (5),

B) on the at least one layer (10), a mask structure (20) with a first (20A) and second structure (2OB) is generated,

C) the at least one layer (10) is structured using an isotropic process,

D) the at least one layer (10) is then structured using an anisotropic process.

2. Process as per the preceding claim to generate at least two structured layers (10A, 15A) which are arranged on top of each other on a substrate (5),

- wherein, in process step A), the first layer (10) and over this, at least one second layer (15) are arranged,
- wherein, in process step C), a second layer (15) and in process step D) the first layer (10) are structured.

3. Process as per one of the preceding claims,

- wherein the first structure of the mask structure is a rough structure and the second structure of the mask structure is a fine structure, wherein the smallest expansion of the rough structure is at least twice as large as the smallest expansion of the fine structure.

4. Process as per one of the claims 2 and 3,

- wherein, in process step C), an etching agent which is selective for the second layer is utilized.

5. Process as per one of the preceding claims,

- wherein, in process step A), metal layers are generated as the first and / or second layers.

6. Process as per the preceding claim,

- wherein, in process step A), a Pt layer is generated on the substrate as the first layer and an Au layer is generated on the substrate as a second layer.

7. Process as per one of the preceding claims, wherein, in process step B), a photoresist layer is generated and structured by means of photolithography into a mask structure.

8. Process as per one of the claims 2 to 7,

- wherein, in step C), the second layer below the mask structure is removed
- wherein, subsequently in a process step C1), the mask structure is lowered onto the first layer in areas in which the second layer beneath the mask structure was removed.

9. Process as per one of the claims 2 to 8,

- wherein, in process step C), the second layer is structured by means of wet chemical isotropic etching,
- wherein, in process step D), the first layer is structured by means of anisotropic dry etching processes.

P2004,0327

10. Process as per one of the preceding claims 2 to 9,

- wherein, in process step C), the second layer is removed except for one or several areas below the mask structure.

11. Process as per one of the preceding claims,

- wherein, in a process step E) which follows D), the mask structure (20) is removed.

12. Process as per one of the preceding claims 2 to 11, for the production of an electrical component (1), wherein

- in process step A), the substrate (5) with its additional functional layers (36, 40, 45, 50) is provided below the first layer (10) ,wherein, the first and second layers (10, 15), respectively, are formed as metal layers,

- in process step B), a mask structure (20) with at least one geometrically formed area (20A) is generated as the first structure, with line-formed structured (20B) originating from it as the second structure,

- in process step C), the second layer (15) is structured into an area (15A) which lies below the at least single geometrically formed area (20A) of the mask structure (20),wherein a bond pad (25) is formed,

- in process step D), the line-formed structures(20B) of the mask structure (20) are transferred into the first layer (10), wherein contact lines (30) are formed,

- wherein the bond pad (25) possesses a form (25B) which is largely adapted to the geometric form (20A) of the geometrically formed area of the

mask structure and a cross section (25C) which widens towards the substrate.

13. Process as per the preceding claim,

- wherein the line-formed structures (20B) of the mask structure (20) are formed in grate arrangements.

14. Electrical component (1) with

- a substrate (5),
- wherein at least a first (15A) and a second (10A) structure are arranged on the substrate (5),
- wherein the first structure is structured by means of an isotropic structuring process, and the second layer is formed by means of an anisotropic structuring process out of at least a single layer (10).

15. Electrical component as per the preceding claim,

- wherein the first (15A) and second (10A) structure are structured from differing first (10) and second (15) layers.

16. Electrical component as per the preceding claim,

- wherein the first structure has a bond pad (25) and the second structure has contact lines.

17. Electrical component as per the preceding claim, formed as a surface wave component,

- in which the contact lines are electrically conducting microstructures and
- the substrate includes a piezoelectric crystal.

18. Component as per claim 16,

- wherein the contact lines (30) are formed in a grate.

19. Component as per one of the claims 16 to 18,

- in which the contact lines (30) include a first electrically conducting material and
- the bond pad (25) includes a first and second electrically conducting layer, wherein the first layer includes the first electrically conducting material, and the second layer includes the second electrically conducting material.

20. Electrical component as per the preceding claim,

- in which the first electrically conducting material is Pt, and the second electrically conducting material is Au.

21. Component as per one of the claims 14 to 20,

- wherein the substrate additionally includes active layers (36, 40, 45, 50).

22. Component (1), formed as an LED as per the preceding claim,

- in which the active layers (36, 40, 45, 50) include p- and n- endowed semiconductor layers (36, 40).

23. Process as per one of the claims 1 to 13,

- wherein, in process step C), the first structure of the mask structure, and in process step D), the second structure of the mask structure are transferred into the at least single layer.

24. Process as per the preceding claim,

- wherein, in process step C), only the first structure, and in process step D), only the second layer is transferred into the at least single layer.

25. Electrical component (1),
- including a substrate (5) with a first (15A) and second structure (10A) arranged thereon,
- wherein the first structure (15A) possesses a cross section (15C) which widens towards the substrate (5) and a geometric form (25B) whose circumference possesses additional recessed areas (25A).

26. Electrical component (1) as per the preceding claim,

- wherein the first structure is a rough structure and the second structure is a fine structure, wherein the smallest extension of the rough structure is at least twice as large as the smallest extension of the fine structure.

27. Electrical component as per one of the claims 25 or 26,
- wherein the first structure may, for instance, consist of a bond pad (25), and the second structure of contact lines (30).